UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,165	12/27/2000	Nigel C. Paver	884.A96US1	5048

45457 7590 09/22/2008

SCHWEGMAN, LUNDBERG & WOESSNER/Intel
PO BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
09/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/748,165	PAVER, NIGEL C.	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-14,16 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-14,16 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/15/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 6-9, 11-14, 16, and 23-25 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and IDS as received on 7/15/2008.

Claim Objections

3. Claims 1 and 23 are objected to because the N-bit word is unclear. In lines 2-3 of claim 1, for instance, applicant claims that the data items of varying field sizes are stored within N-bit words, and in lines 4-5, applicant claims that the same N-bit words comprise arithmetic flags. Is this correct? Does a single N-bit word comprise both flags and data items? Clarification is requested.

4. Claims 3 and 8 are objected to because of the following informalities: Applicant's use of the word "either" is grammatically correct, as "either" is used when referring to one of only two entities. Since applicant is claiming that a field size could be more than two items, applicant should replace "either" with --one of-- or --any of--. Or, applicant could simply delete "either". Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 6-9, 11-14, 16, and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Golston, U.S. Patent No. 6,026,484.

7. Referring to claim 1, Golston has taught a device to manage a plurality of arithmetic flags, wherein an M-bit set of arithmetic flags is associated with each of a plurality of data items of varying field sizes within words of N-bits (see column 19, lines 1-46, column 20, lines 46-50, column 21, lines 56-67, and Table 4 in column 22), M and N being positive integers, comprising: a combination function module to examine one of the N-bit words comprising a plurality of sets of arithmetic flags, to determine a data item field size for the word, and based on the determination of the data item field size to logically combine the plurality of arithmetic flags of the sets within the word into a single combined arithmetic flag variable of M bits, wherein, in combining, the combination function module performs an OR operation (see column 19, lines 14-22 and lines 38-46), wherein the plurality of arithmetic flags represent a result status of the plurality of data items after a mathematical operation is performed by a processor on the plurality of data items. Essentially, an arithmetic operation may be performed on multiple data items at once. For instance, if there are four data items to operate on, then four arithmetic flags will be set in register 211 (Fig.5). Then, the four sets of arithmetic flags are combined into one set (through AND/OR operations) and the combined result is stored in the flag section of register 210 (Fig.5 and Fig.6). Note that the data size of the word is determined based on the ASIZE field of register 210 (column 20, lines 34-35).

8. Referring to claim 2, Golston has taught the device recited in claim 1, further comprising a condition check module that determines the result status of the combined arithmetic flag variable and causes the processor to execute an appropriate operation based on the status. See column 5, lines 39-40. Note that the status bits are checked to control conditional execution.

9. Referring to claim 3, Golston has taught the device recited in claim 1, wherein the field size is based on either a nibble, byte, half-word, or word in length. See column 20, Table 2, and lines 38-45).

10. Referring to claim 4, Golston has taught the device recited in claim 3, wherein the plurality of arithmetic flags further comprise a negative data value, a zero data value, a carry out occurrence in a data value, or an overflow condition in a data item in the plurality of data items. See Fig.6 and column 19, lines 1-46.

11. Referring to claim 6, Golston has taught the device recited in claim 2, wherein the result status determined by the condition further comprises:

a) any data item has overflowed. See column 19, lines 23-37, and note that if the V bit set, overflow is detected.

b) any data item has not overflowed. See column 19, lines 23-37, and note that if the V bit is clear, overflow is not detected.

c) any data item is positive or zero. See column 19, lines 1-13, and note that if the N bit is clear, a positive or zero data item is detected.

d) any data item is negative. See column 19, lines 1-13, and note that if the N bit is set, a positive or zero data item is detected.

e) any data item is zero. See column 19, lines 38-46, and note that if the Z bit is set, a zero data item is detected.

f) any data item is not zero. See column 19, lines 38-46, and note that if the Z bit is clear, a zero data item is detected.

g) any data item has a carry out. See column 19, lines 14-22, and note that if the C bit is set, a carry is detected.

h) any data item does not have a carry out. See column 19, lines 14-22, and note that if the C bit is clear, a carry is not detected.

i) all data items have overflowed. See column 19, lines 23-37, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so overflow of all data items can be checked.

j) all data items have not overflowed. See column 19, lines 23-37, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so non-overflow of all data items can be checked.

k) all data items are positive or zero. See column 19, lines 1-13, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are zero or positive.

l) all data items are negative. See column 19, lines 1-13, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so negativity of all data items can be checked.

m) all data items are zero. See column 19, lines 38-46, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are zero.

n) all data items are not zero. See column 19, lines 38-46, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are non-zero.

o) all data items have a carry out. See column 19, lines 14-22, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so carry out of all data items can be checked.

p) all data items do not have a carry out. See column 19, lines 14-22, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so non-carry out of all data items can be checked.

12. Referring to claim 7, Golston has taught a method of combining a plurality of arithmetic flags for presentation to a processor, comprising:

a) determining a field size of the plurality of arithmetic flags on which to base a combination process, wherein the plurality of arithmetic flags represent a result status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items. See column 19, lines 1-46, column 20, lines 46-50, column 21, lines 56-67, and Table 4 in column 22.

b) extracting the plurality of arithmetic flags based on the field size and logically combining the plurality of arithmetic flags based on a function selected when a combination process is selected, wherein the function comprises an OR operation. See column 19, lines 14-22 and lines 38-46.

d) storing a result of the combining of the plurality of arithmetic flags in a destination register for access by the processor. See column 19, lines 14-22 and lines 38-46. Essentially, an arithmetic operation may be performed on multiple data items at once. For instance, if there are four data items to operate on, then four arithmetic flags will be set in register 211 (Fig.5). Then, the four

sets of arithmetic flags are combined into one set (through AND/OR operations) and the combined result is stored in the flag section of register 210 (Fig.5 and Fig.6). Note that the data size of the word is determined based on the ASIZE field of register 210 (column 20, lines 34-35).

13. Referring to claim 8, Golston has taught a method as described in claim 7. Furthermore, claim 8 is rejected for the same reasons set forth in the rejection of claim 3.

14. Referring to claim 9, Golston has taught a method as described in claim 8. Furthermore, claim 9 is rejected for the same reasons set forth in the rejection of claim 4.

15. Referring to claim 11, Golston has taught a method as described in claim 7. Furthermore, claim 11 is rejected for the same reasons set forth in the rejection of claim 6.

16. Referring to claim 12, Golston has taught an apparatus comprising a data storage medium for storing instructions, wherein the instructions, when executed by a processor, result in the processor performing a method, the method comprising:

a) determining a field size of the plurality of arithmetic flags on which to base a combination process, wherein the plurality of arithmetic flags represent the status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items. See column 19, lines 1-46, column 20, lines 46-50, column 21, lines 56-67, and Table 4 in column 22.

b) extracting the plurality of arithmetic flags based on the field size and logically combining the plurality of arithmetic flags based on a function selected when a combination process is selected, wherein the function comprises an OR operation. See column 19, lines 14-22 and lines 38-46.

d) storing a result of the combining of the plurality of arithmetic flags in a destination register for access by the processor. See column 19, lines 14-22 and lines 38-46. Essentially, an arithmetic

operation may be performed on multiple data items at once. For instance, if there are four data items to operate on, then four arithmetic flags will be set in register 211 (Fig.5). Then, the four sets of arithmetic flags are combined into one set (through AND/OR operations) and the combined result is stored in the flag section of register 210 (Fig.5 and Fig.6). Note that the data size of the word is determined based on the ASIZE field of register 210 (column 20, lines 34-35).

17. Referring to claim 13, Golston has taught an apparatus as described in claim 12. Furthermore, claim 13 is rejected for the same reasons set forth in the rejection of claim 3.

18. Referring to claim 14, Golston has taught an apparatus as described in claim 13. Furthermore, claim 14 is rejected for the same reasons set forth in the rejection of claim 4.

19. Referring to claim 16, Golston has taught an apparatus as described in claim 12. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 6.

20. Referring to claim 23, Golston has taught a system to manage a plurality of arithmetic flags, wherein an M-bit set of arithmetic flags is associated with each of a plurality of data items of varying field sizes within words of N bits (see column 19, lines 1-46, column 20, lines 46-50, column 21, lines 56-67, and Table 4 in column 22), M and N being positive integers, comprising: a) a combination function module to examine one of the N-bit words comprising a plurality of sets of arithmetic flags and to determine a data item field size for the word, and based on the determination of the data item field size to logically combine the plurality of arithmetic flags of the sets within the word into a single combined arithmetic flag variable of M bits, wherein, in combining, the combination function module performs an OR operation (see column 19, lines 14-22 and lines 38-46), wherein the plurality of arithmetic flags represent a result status of the plurality of data items after a mathematical operation is performed by a processor on the plurality

of data items. Essentially, an arithmetic operation may be performed on multiple data items at once. For instance, if there are four data items to operate on, then four arithmetic flags will be set in register 211 (Fig.5). Then, the four sets of arithmetic flags are combined into one set (through AND/OR operations) and the combined result is stored in the flag section of register 210 (Fig.5 and Fig.6). Note that the data size of the word is determined based on the ASIZE field of register 210 (column 20, lines 34-35).

b) a processor including a condition check module coupled to the combination function module, the processor to receive the single combined arithmetic flag variable and to determine the next operation to perform based upon the result status of the single combined arithmetic flag variable. See column 5, lines 39-40. Note that the status bits are checked to control conditional execution.

21. Referring to claim 24, Golston has taught the system of claim 23, wherein the processor includes at least three stages of pipelining. See Fig.4.

22. Referring to claim 25, Golston has taught the system of claim 24, wherein the at least three stages of pipelining include a fetch stage, a decode stage, and an execute stage. See Fig.4, and note the fetch and execute stages. In between is a decode stage, which accepts fetched instructions, decodes them, and sends the execution unit the appropriate signals. See Fig.5, component 250.

Response to Arguments

23. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183
August 27, 2008